Amendments to the Claims:

The following listing of Claims will replace all prior versions, and listings, of claims in the application:

1. (Original) A structure in a phase changeable memory cell, comprising:

a bottom electrode having an interlayer dielectric layer thereon, the bottom electrode having a recess therein that extends beyond a boundary between the bottom electrode and the interlayer dielectric; and

a phase changeable layer in the recess including a protruding potion of the phase changeable layer that protrudes into the bottom electrode beyond the boundary.

2. (Original) A structure according to Claim 1 wherein the recess extends beyond the boundary by a depth to define a side wall of the recess that contacts the protruding portion of the phase changeable layer, wherein the depth is defined to limit an amount of heat transmission from the bottom electrode to the phase changeable layer across the side wall to less than an amount sufficient to cause the phase changeable layer to change phase between a crystalline state and an amorphous state.

3. (Original) A structure according to Claim 1 wherein the interlayer dielectric layer includes a contact hole with the phase changeable layer therein on the recess.

4. (Original) A structure according to Claim 3 wherein the contact hole has an inward tapered profile extending toward the bottom electrode that defines an opening that is narrower at in the recess than away from the recess.

5. (Original) A phase changeable memory cell, comprising:

bottom electrodes disposed over the semiconductor substrate;

a interlayer dielectric layer formed over the semiconductor substrate having the

bottom electrodes; and

a plurality of data storage elements extended through the interlayer dielectric layer to connect with the bottom electrodes, respectively,

wherein, each data storage elements is extended into the bottom electrode to predetermined depth so that a portion of the sidewall of the data storage element is contact with the bottom electrode.

6. (Original) The phase changeable memory cell of claim 5, further comprising:

a lower interlayer dielectric layer disposed over the semiconductor substrate; and

storage node plugs extended through the lower interlayer dielectric layer to connect with predetermined region of the semiconductor substrate,

wherein the bottom electrode is formed on the storage node plug to connect with the storage node plug.

7. (Original) The phase changeable memory cell of claim 5, further comprising:

a lower interlayer dielectric layer disposed over the semiconductor substrate,

wherein the bottom electrode is extended through the lower interlayer dielectric layer to contact with directly the semiconductor substrate.

8. (Original) The phase changeable memory cell of claim 5,

the bottom electrode is formed of one selected form group comprising titanium nitride (TiN), titanium aluminum nitride (TiAlN), titanium silicon nitride (TiSiN), tantalum aluminum nitride (TaAlN) and tantalum silicon nitride (TaSiN).

9. (Original) The phase changeable memory cell of claim 5, the data storage element comprising:

a phase changeable pattern electrically connected with the bottom electrode; and

an upper electrode formed on the phase changeable pattern.

10. (Original) The phase changeable memory cell of claim 9,

the upper electrode is formed of one selected form group comprising titanium nitride (TiN), titanium aluminum nitride (TiAlN), titanium silicon nitride (TiSiN), tantalum aluminum nitride (TaAlN) and tantalum silicon nitride (TaSiN).

Claims 11-23 (Canceled).

24. (Original) A structure in a phase changeable memory cell, comprising:

a bottom electrode having an interlayer dielectric layer thereon; and

a phase changeable layer extending through the interlayer dielectric layer and protruding into a recess in the bottom electrode.